

FORM PTO-1449 U.S. Department of Commerce
Patent and Trademark Office

Attorney Docket Number
5646-113

Serial No.
10/648,090

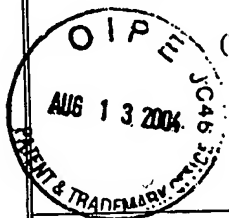
LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

Applicants: Declan McDonagh et al.

Filing Date: August 26, 2003

Group
2816



U. S. PATENTS & PATENT APPLICATION PUBLICATIONS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
<i>W</i>	1	6,539,072	03-25-03	Donnelly et al.	375	371	
<i>W</i>	2	6,125,157	09-26-00	Donnelly et al.	375	371	
<i>W</i>	3	5,614,855	03-25-97	Lee et al.	327	158	
<i>W</i>	4	5,485,490	5,485,490	Leung et al.	375	371	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>W</i>	5	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496					

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Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

9/3/04

8/27/03

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U. S. PATENTS & PATENT APPLICATION PUBLICATIONS							
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
W	1	6,597,212	7/22/03	Wang et al.	327	117	
W	2	6,525,584	2/25/03	Seo et al.	327	276	
	3	6,509,773	1/21/03	Buchwald et al.	327	248	
	4	6,466,098	10/15/02	Pickering	331	25	
	5	6,433,645	8/13/02	Mann et al.	331	18	
	6	6,388,478	5/14/02	Mann	327	113	
	7	6,384,653	5/7/02	Broome	327	247	
	8	6,359,486	3/19/02	Chen	327	231	
	9	6,329,859	12/11/01	Wu	327	291	
W	10	6,271,702	8/7/01	Stansell	327	295	
W	11	6,111,445	8/29/00	Zerbe et al.	327	231	
FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation Yes No		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
12	Rabaey, Jan M., "Synchronization at the System Level," Digital Integrated Circuits, A Design Perspective, Prentice-Hall, Inc., pp. 540-543 NO DATE IS PROVIDED						
W	13	"High Speed Multi-Phase PLL Clock Buffer," Cypress Semiconductor Corporation, Revised July 25, 2003, 14 pages					

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